Doc. Number :

☐ Tentative Specification
☐ Preliminary Specification
■ Approval Specification

MODEL NO.: G121XCE
SUFFIX: L02

Customer:

APPROVED BY **SIGNATURE**

Name / Title
Note

Please return 1 copy for your confirmation with your signature and comments.

Approved By	Checked By	Prepared By
陳立錚	林秋森	許秝茵

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REVISION HISTORY

Version	Date	Page	Description
3.0	Jan 9 , 2019	All	Spec Ver.3.0 was first issued.
3.1	Feb 15,2019	P28	10.1 MODULE LABEL Add NBINX FAB ID: COCKN
3.2	Apr 11, 2019	P19	6.3 The Input Data Format Modify figure (delete “NC”)
3.3	May 4, 2021	P5	Modify 1.4 GENERAL SPECIFICATI0NS
		P6	Modify 1.5 MECHANICAL SPECIFICATIONS
		P7	Modify 2. ABSOLUTE MAXIMUM RATINGS Note(2)
		P8	Modify 2.2.1 TFT LCD MODULE
		P9	Modify 3.1 TFT LCD MODULE
		P10	Modify 3.2 BACKLIGHT UNIT
		P17	Modify 6. INTERFACE TIMING
		P20	Modify 6.2 POWER ON/OFF SEQUENCE Note(1)~Note(7)
		P23-P24	Add 7.2 OPTICAL SPECIFICATIONS Definition & Modify Note(2)~Note(6)
		P26	Modify 8. RELIABILITY TEST CRITERIA
		P29	Modify 10. DEFINITION OF LABELS
		P30-P31	Modify 11. PRECAUTIONS
		P34-P40	Add Appendix
3.4	May 27, 2021	P25	Modify 7.2 OPTICAL SPECIFICATIONS Definition Add some definition of module placement in Note(5)

1. GENERAL DESCRIPTION

1.1 OVERVIEW

The G121XCE-L02 model is a 12.1" TFT-LCD IAV module with a white LED Backlight Unit and a 20-pin 1ch-LVDS interface. This module supports 1024 x 768 XGA mode and displays 262k/16.7M colors. The converter for the Backlight Unit is built in.

1.2 FEATURES

- Wide viewing angle
- High contrast ratio
- XGA (1024 x 768 pixels) resolution
- Wide operating temperature
- DE (Data Enable) mode
- LVDS (Low Voltage Differential Signaling) interface
- Reversible-scan direction
- RoHS Compliance

1.3 APPLICATION

- TFT LCD Monitor
- Industrial Application
- Amusement

1.4 GENERAL SPECIFICATI0NS

Item	Specification	Unit	Note
Active Area	245.76(H) x 184.32(V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1024 x R.G.B. x 768	pixel	-
Pixel Pitch	0.240(H) x 0.240(V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	262k/16.7M	color	-
Transmissive Mode	Normally black / AAS	-	-
Surface Treatment	Hard coating (3H), Anti-Glare	-	-
Module Power Consumption	10.12W (white pattern)	W	Typ

1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal(H)	260	260.5	261	mm	(1)
	Vertical(V)	203.5	204	204.5	mm	
	Depth(D)	7.9	8.4	8.9	mm	
Bezel Area	Horizontal	248.5	249	249.5	mm	-
	Vertical	187	187.5	188	mm	
Active Area	Horizontal	-	245.76	-	mm	
	Vertical	-	184.32	-	mm	
Weight		-	490	510	g	

Note (1)Please refer to the attached drawings for more information of front and back outline dimensions.

2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Operating Ambient Temperature	T_{OP}	-30	+70	ºC	(1)(2)
Storage Temperature	T_{ST}	-40	+80	ºC	

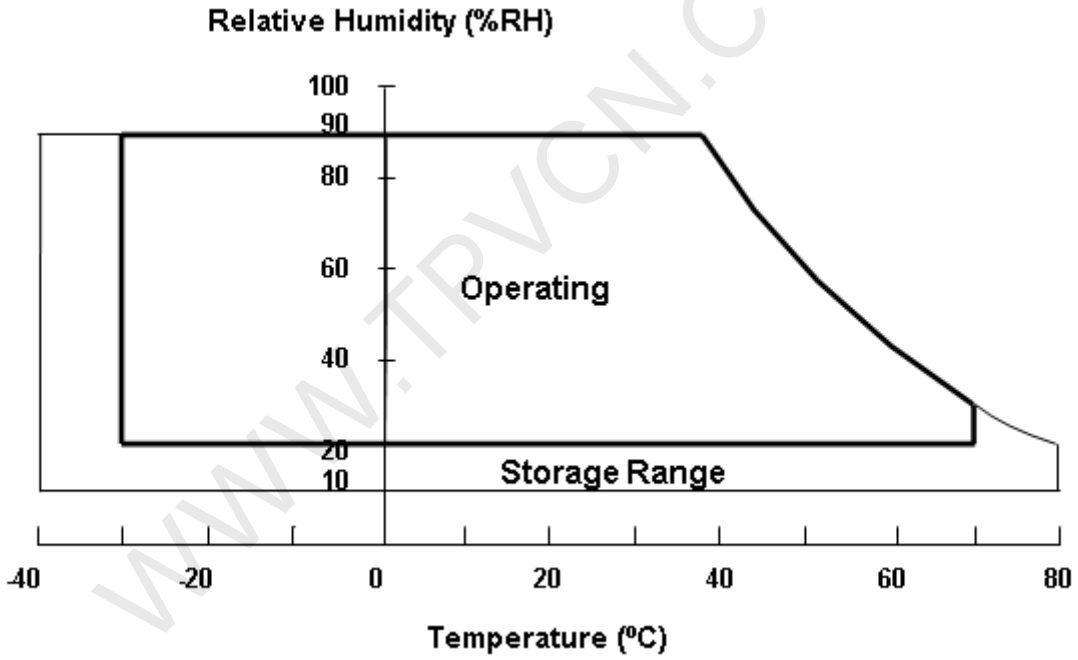
Note (1)

(a) 90 %RH Max.

(b) Wet-bulb temperature should be 39 ºC Max.

(c) No condensation.

Note (2)Panel surface temperature should be 0℃ min. and 65℃ max under Vcc=5.0V, fr =60Hz, typical LED string current, 25℃ ambient temperature, and no humidity control . Any condition of ambient operating temperature ,the surface of active area should be keeping not higher than 65℃.



2.2 ELECTRICAL ABSOLUTE RATINGS

2.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCC	-0.3	3.6	V	(1)
Logic Input Voltage	V_{IN}	-0.3	3.6	V	

2.2.2 BACKLIGHT UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Converter Voltage	V_i	-0.3	18	V	(1) , (2)
Enable Voltage	EN	---	5.5	V	
Backlight Adjust	Dimming	---	5.5	V	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) Specified values are for lamp (Refer to 3.2 for further information).

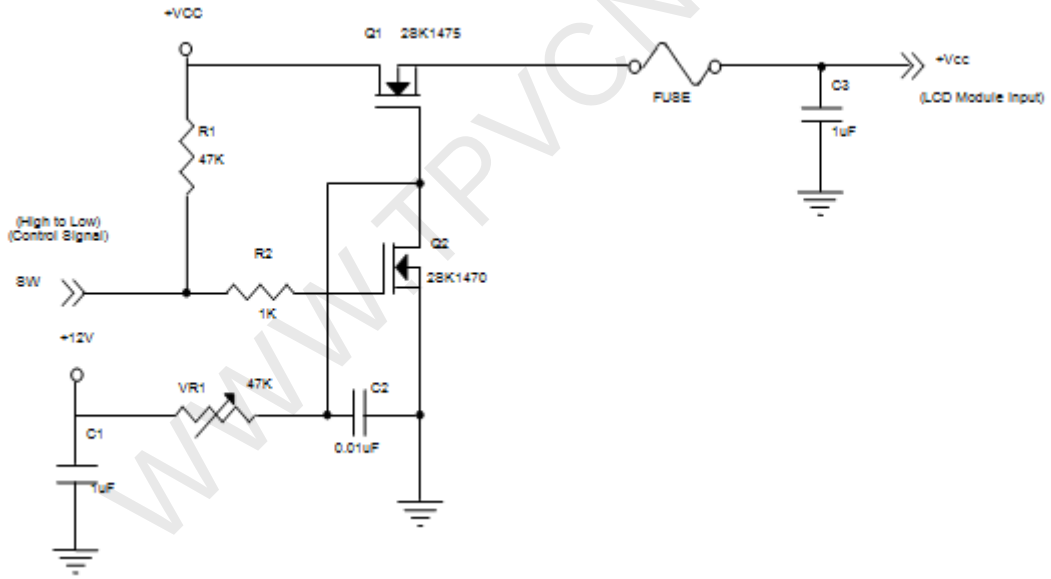
3. ELECTRICAL CHARACTERISTICS

3.1 TFT LCD MODULE

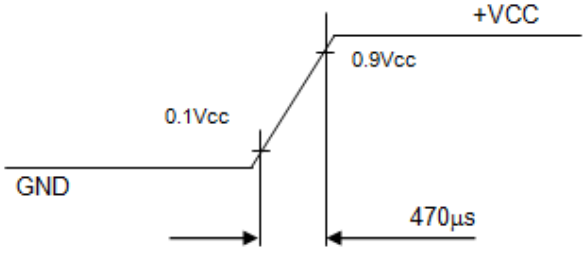
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{CC}	3.15	3.3	3.45	V	-
Ripple Voltage		V_{RP}	-	-	200	mVp-p	
Inrush Current		I_{INRUSH}	-	-	4	A	(2)
Power Supply Current	White	Icc	-	520	620	mA	(3)a
	Black		-	420	510	mA	(3)b
LVDS differential input voltage		V_{id}	100	-	600	mV	
LVDS common input voltage		V_{ic}	1.0	1.2	1,4	V	
Differential Input Voltage for LVDS Receiver Threshold	"H" Level	V_{IH}	+100	-	-	mV	-
	"L" Level	V_{IL}	-	-	-100	mV	-
Terminating Resistor		R_T	-	100	-	Ohm	-

Note (1)The module should be always operated within above ranges.

Note (2)Measurement Conditions:



Vcc rising time is 470µs



Note (3) The specified power supply current is under the conditions at Vcc = 3.3V, Ta = 25 ± 2 ºC, f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

a. White Pattern

Active Area

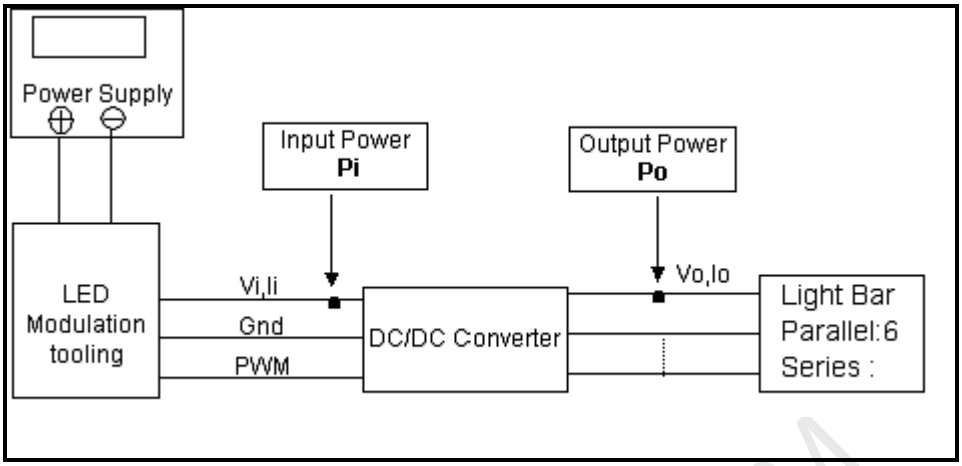
b. Black Pattern

Active Area

3.2 BACKLIGHT UNIT

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Converter Input Voltage		Vi	10.8	12.0	13.2	VDC	(Duty 100%)
Converter Input Ripple Voltage		ViRP	-	-	500	mV	
Converter Input Current		Ii	-	0.7	0.85	ADC	@ Vi = 12V (Duty 100%)
Converter Inrush Current		IiRUSH	-	-	3.0	A	@ Vi rising time=20ms (Vi=12V)
Input Power Consumption		Pi	-	8.4	10.2	W	(1)
EN Control Level	Backlight on	ENLED (BLON)	2.5	3.3	5.0	V	
	Backlight off		0	---	0.3	V	
PWM Control Level	PWM High Level	Dimming (E_PWM)	2.5	3.3	5.0	V	
	PWM Low Level		0	-	0.15	V	
PWM Noise Range		VNoise	-	-	0.1	V	
PWM Control Frequency		fPWM	190	200	20k	Hz	(2)
PWM Control Duty Ratio		-	5		100	%	(2), @ 190Hz< f_{PWM} <1kHz
			20	-	100	%	(2), @ 1kHz≦f_{PWM} <20kHz
LED Life Time		LLED	30,000	-	-	Hrs	(3)

Note (1)LED current is measured by utilizing a high frequency current meter as shown below:



Note (2) At 190 ~1kHz PWM control frequency, duty ratio range is restricted from 5% to 100%.

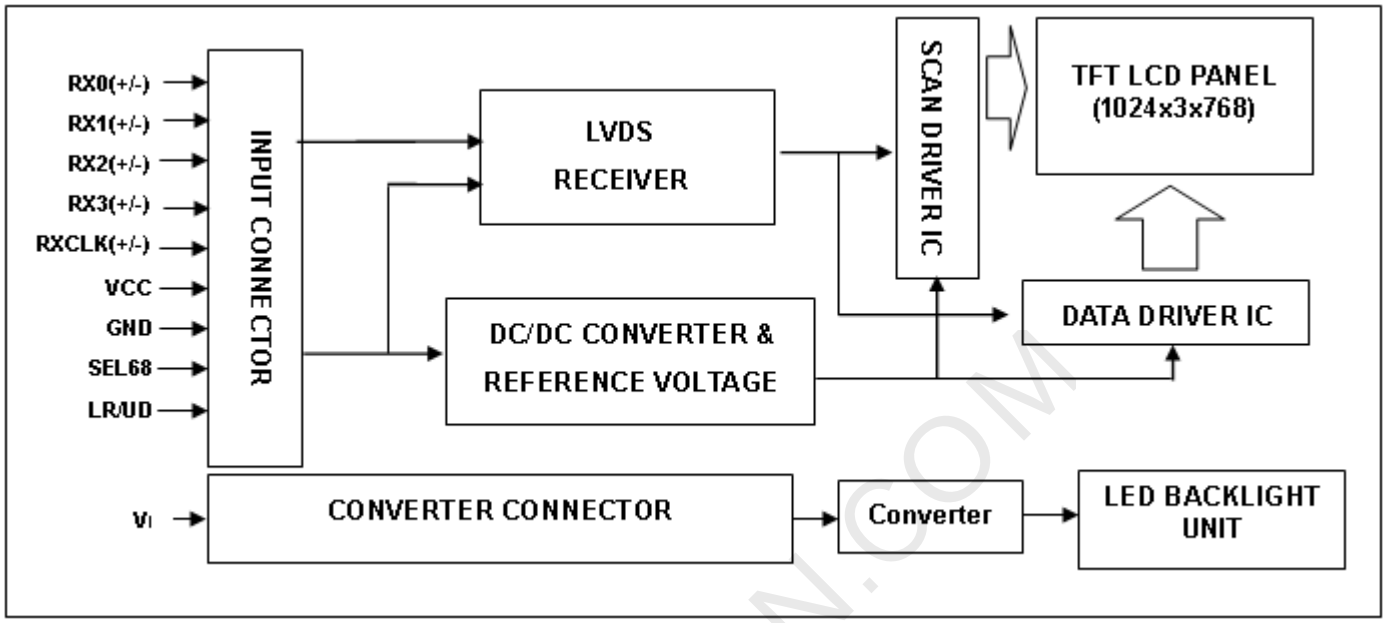
1K ~20kHz PWM control frequency, duty ratio range is restricted from 20% to 100%.

If PWM control frequency is applied in the range from 1KHz to 20KHZ, The “non-linear” phenomenon on the Backlight Unit may be found. So It’s a suggestion that PWM control frequency should be less than 1KHz.

Note (3)The lifetime of LED is estimated data and defined as the time when it continues to operate under the conditions at Ta = 25 ±2 ºC and Duty 100% until the brightness becomes ≦ 50% of its original value. Operating LED at high temperature condition will reduce life time and lead to color shift.

4. BLOCK DIAGRAM

4.1 TFT LCD MODULE



5. INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD MODULE

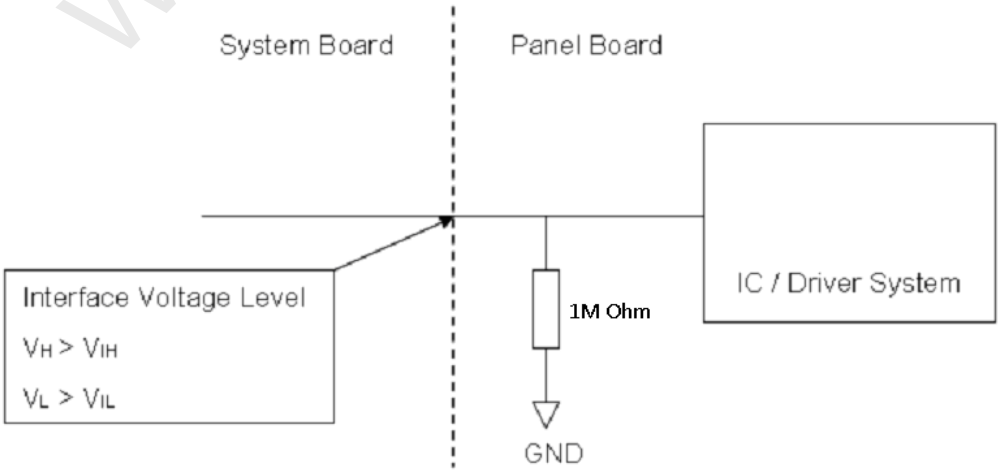
Pin	Name	Description	Remark
1	RX3+	Differential Data Input, CH3 (Positive)	
2	RX3-	Differential Data Input, CH3 (Negative)	
3	NC	NC	
4	SEL68	LVDS 6/8 bit select function control, Low → 6 bit Input Mode High → 8bit Input Mode	Note (3) (4)
5	GND	Ground	
6	RXC+	Differential Clock Input (Positive)	
7	RXC-	Differential Clock Input (Negative)	
8	GND	Ground	
9	RX2+	Differential Data Input , CH2 (Positive)	
10	RX2-	Differential Data Input , CH2 (Negative)	
11	GND	Ground	
12	RX1+	Differential Data Input , CH1 (Positive)	
13	RX1-	Differential Data Input, CH1 (Negative)	
14	GND	Ground	
15	RX0+	Differential Data Input, CH0 (Positive)	
16	RX0-	Differential Data Input, CH0 (Negative)	
17	reLR	Horizontal Reverse Scan Control, Low → Normal Mode. High → Horizontal Reverse Scan	Note (3) (4)
18	reUD	Vertical Reverse Scan Control, Low → Normal Mode, High → Vertical Reverse Scan	Note (3) (4)
19	VCC	Power supply	
20	VCC	Power supply	

Note (1) Connector Part No.: P-TWO 187191-20101-3 or STARCONN 076B20-0048RA-G4 or equivalent.

Note (2) User's connector Part No.: JAE FI-SE20ME or equivalent.

Note (3) "Low" stands for 0V. "High" stands for 3.3V.

Note (4) SEL68, reLR, reUD



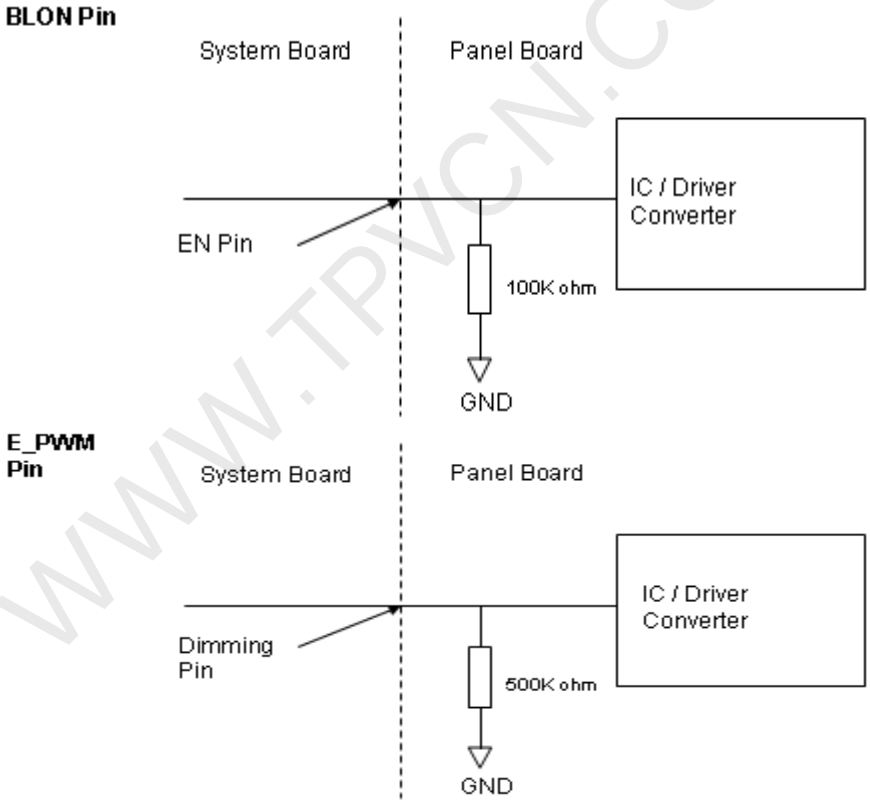
5.2 BACKLIGHT UNIT(CONVERTER CONNECTOR PIN)

Pin	Symbol	Description	Remark
1	Vi	Converter input voltage	12V
2	Vi	Converter input voltage	12V
3	Vi	Converter input voltage	12V
4	Vi	Converter input voltage	12V
5	VGND	Converter ground	Ground
6	VGND	Converter ground	Ground
7	VGND	Converter ground	Ground
8	VGND	Converter ground	Ground
9	EN	Enable pin	3.3V, Note (3)
10	ADJ	Backlight Adjust	PWM Dimming (190-210Hz, Hi: 3.3VDC, Lo: 0VDC) , Note (3)

Note (1) Connector Part No.: 91208-01001-H01 (ACES) or equivalent.

Note (2) User's connector Part No.: 91209-01011 (ACES) or equivalent

Note (3) EN(BLON), ADJ(E_PWM) as shown below :



5.3 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 6-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																	
		Red						Green						Blue					
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
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	Green(61)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	Green(62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Gray Scale Of Blue	Blue(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(61)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
	Blue(62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue(63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

Note (1)0: Low Level Voltage, 1: High Level Voltage

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
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	Red(253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green(0)/ Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
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	Green(253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
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	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

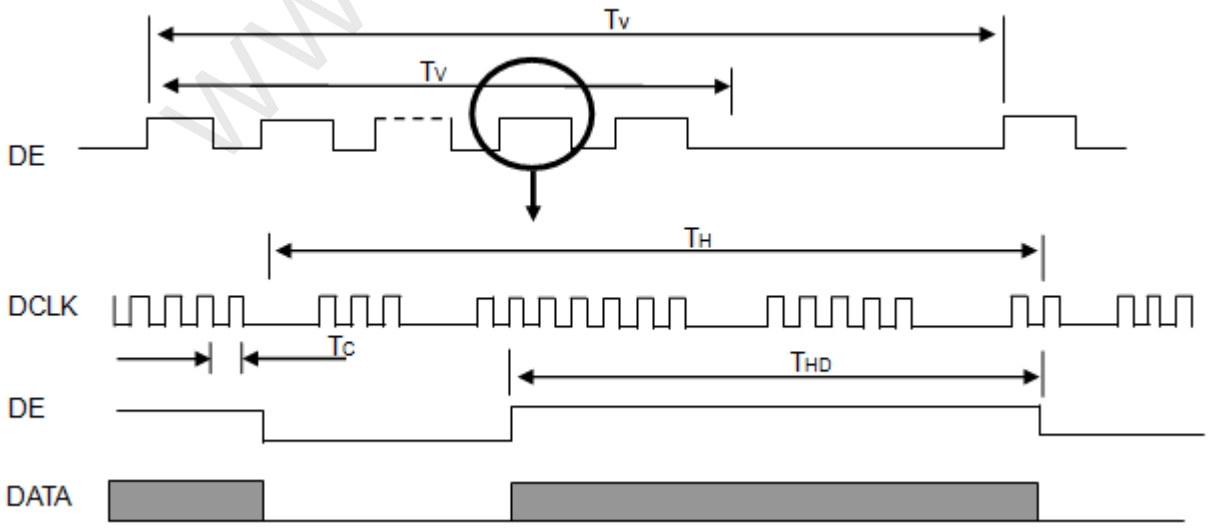
The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Clock	Frequency	Fc	57.7	65	73.6	MHz	-
	Period	Tc	13.6	15.4	17.3	ns	
	Input cycle to cycle jitter	Trcl	---	---	200	ns	(a)
	Input Clock to data skew	TLVCCS	-0.02*Tc	---	0.02*Tc	ps	(b)
	Spread spectrum modulation range	Fclkin_mod	0.987*Fc	---	1.013*Fc	MHz	(c)
	Spread spectrum modulation frequency	FSSM	---	---	200	KHz	
	High Time	Tch	---	4/7	---	Tch	
	Low Time	Tcl	---	3/7	---	Tch	
Vertical Display Term	Frame Rate	Fr	---	60	---	Hz	Tv=Tvd+Tvb
	Total	Tv	776	806	838	Th	-
	Active Display	Tvd	768	768	768	Th	-
	Blank	Tvb	8	38	70	Th	-
Horizontal Display Term	Total	Th	1240	1344	1464	Tc	Th=Thd+Thb
	Active Display	Thd	1024	1024	1024	Tc	-
	Blank	Thb	216	320	440	Tc	-

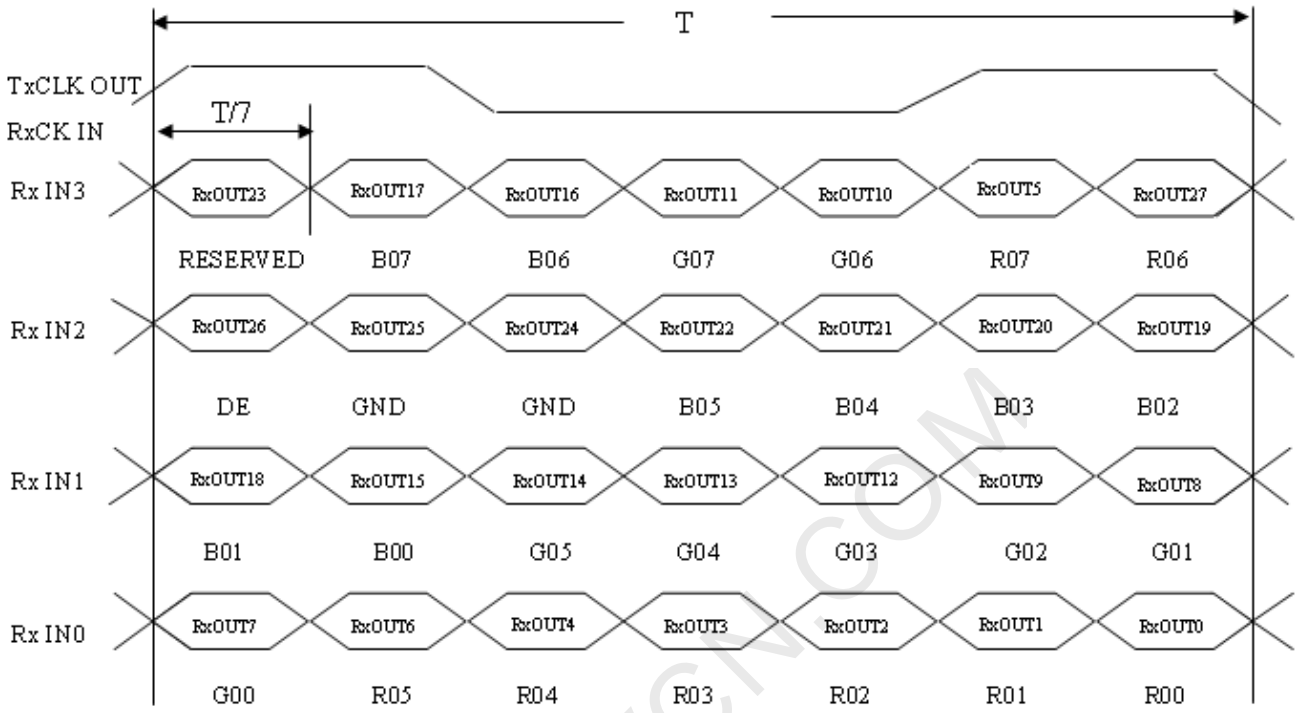
Note (1) Because this module is operated by DE only mode, Hsync and Vsync input signals should be set to low logic level or ground. Otherwise, this module would operate abnormally.

Note (2) The Tv(Tvd+Tvb) must be integer, otherwise, the module would operate abnormally.

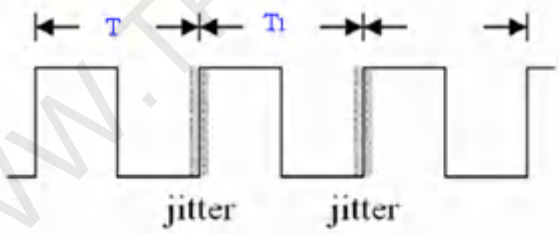
INPUT SIGNAL TIMING DIAGRAM



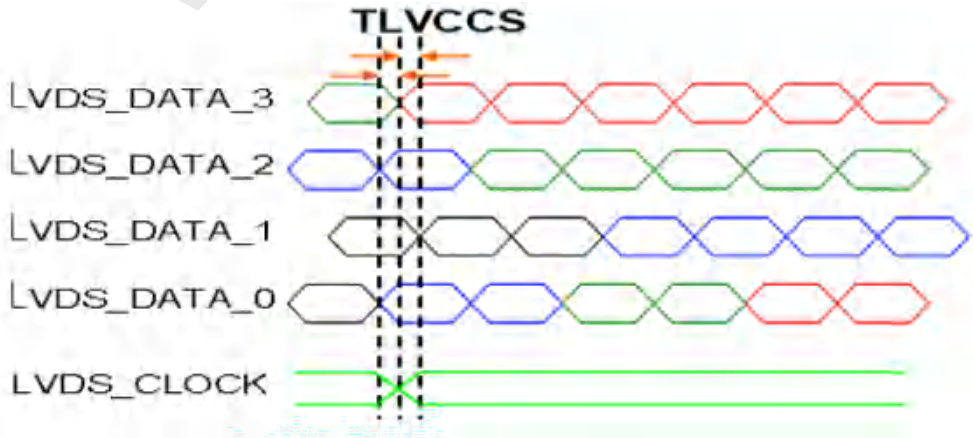
TIMING DIAGRAM of LVDS



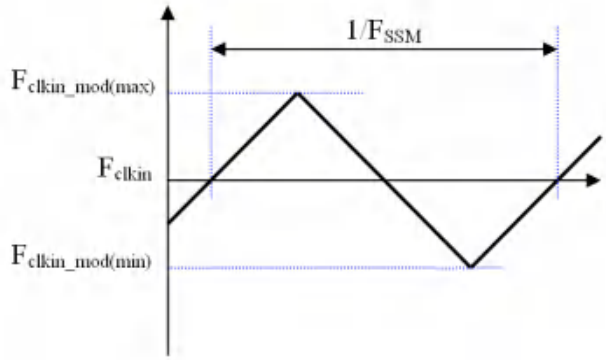
Note (a) The input clock cycle-to-cycle jitter is defined as below figures. Trcl = I T_1 – TI



Note (b) Input Clock to data skew is defined as below figures.

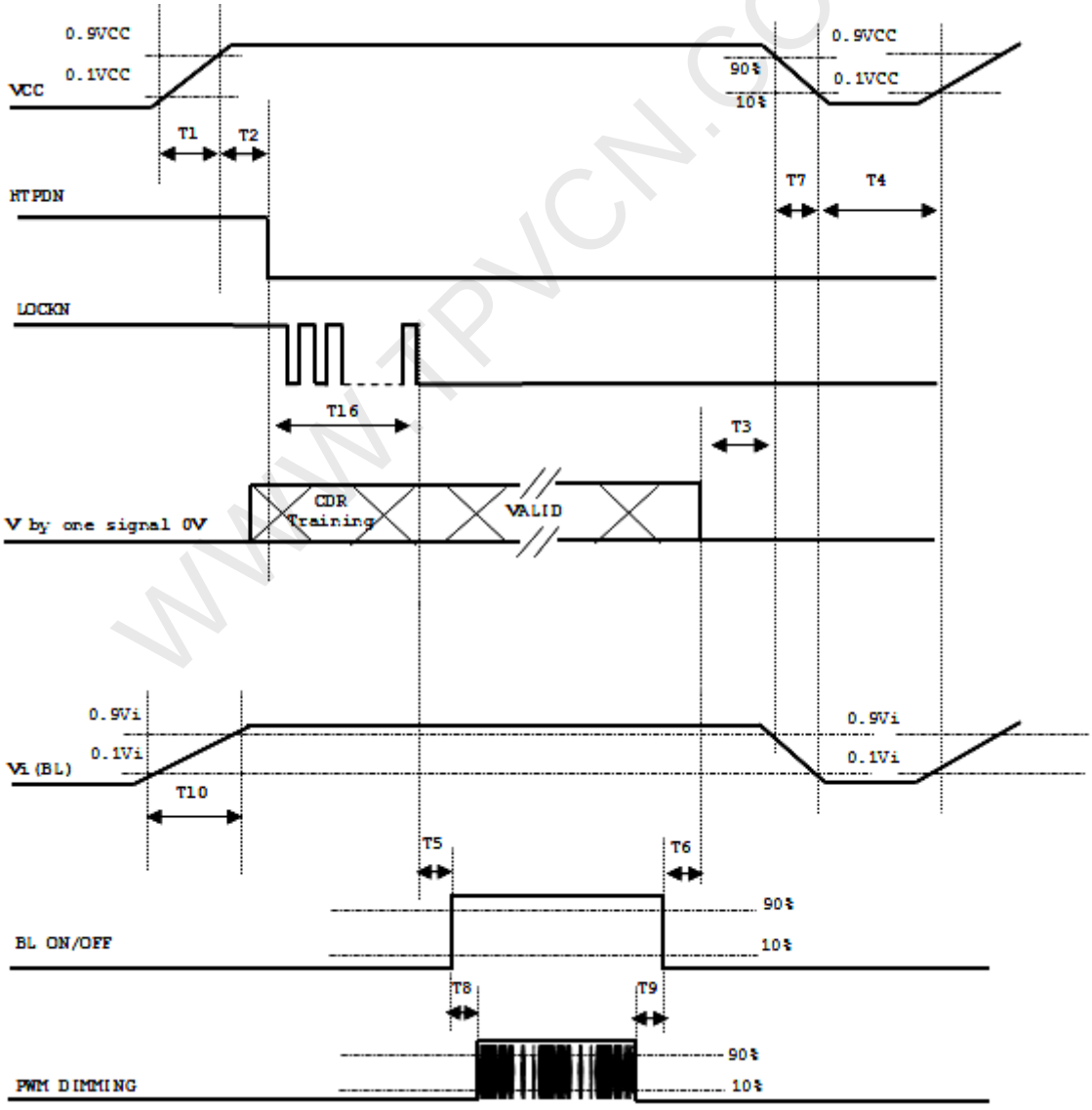


Note (c) The SSCG (Spread spectrum clock generator) is defined as below figures.



6.2 POWER ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD assembly, the power on/off sequence should be as the diagram below.



Parameter	Value			Units
	Min	Typ	Max	
T1	0.5	---	10	ms
T2	0	---	50	ms
T3	0	---	50	ms
T4	500	---	---	ms
T5	450	---	---	ms
T6	200	---	---	ms
T7	10	---	100	ms
T8	10	---	---	ms
T9	10	---	---	ms
T10	20	---	50	ms

Note(1) The supply voltage of the external system for the module input should be the same as the definition of Vcc.

Note(2) When the backlight turns on before the LCD operation of the LCD turns off, the display may momentarily become abnormal screen.

Note(3) In case of VCC = off level, please keep the level of input signals on the low or keep a high impedance.

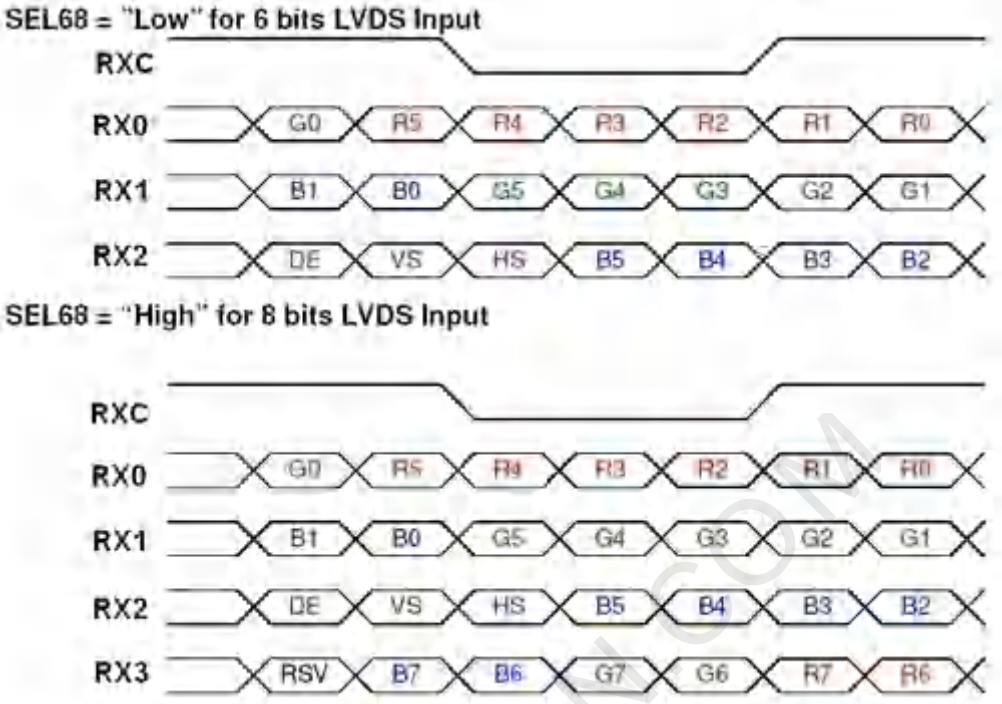
Note(4) T4 should be measured after the module has been fully discharged between power off and on period.

Note(5) Interface signal shall not be kept at high impedance when the power is on.

Note(6) INX won't take any responsibility for the products which are damaged by the customers not following the Power Sequence.

Note(7) There might be slight electronic noise when LCD is turned off (even backlight unit is also off). To avoid this symptom, we suggest "Vcc falling timing" to follow "T7 spec".

6.3 THE INPUT DATA FORMAT



Note (1) R/G/B data 7: MSB, R/G/B data 0: LSB

Note (2) Please follow PSWG

Signal Name	Description	Remark
R7 R6 R5 R4 R3 R2 R1 R0	Red Data 7 (MSB) Red Data 6 Red Data 5 Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB)	Red-pixel Data Each red pixel's brightness data consists of these 8 bits pixel data.
G7 G6 G5 G4 G3 G2 G1 G0	Green Data 7 (MSB) GreenData 6 GreenData 5 GreenData 4 GreenData 3 GreenData 2 GreenData 1 GreenData 0 (LSB)	Green-pixel Data Each green pixel's brightness data consists of these 8 bits pixel data.
B7 B6 B5 B4 B3 B2 B1 B0	Blue Data 7 (MSB) Blue Data 6 Blue Data 5 Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB)	Blue-pixel Data Each blue pixel's brightness data consists of these 8 bits pixel data.
RXCLKIN+ RXCLKIN-	LVDS Clock Input	
DE	Display Enable	
VS	Vertical Sync	
HS	Horizontal Sync	

Note (3) Output signals from any system shall be low or Hi-Z state when VCC is off.

6.4 SCANNING DIRECTION

The following figures show the image see from the front view. The arrow indicates the direction of scan. PCBA on the top side.

Fig.1 Normal Scan

Fig.2 Reverse Scan

Fig.3 Reverse Scan

Fig.4 Reverse Scan

Fig. 1 Normal scan (pin 17, reLR = Low, pin 18, reUD = Low)

Fig. 2 Reverse scan (pin 17, reLR = High, pin 18, reUD = Low)

Fig. 3 Reverse scan (pin 17, reLR = Low, pin 18, reUD = High)

Fig. 4 Reverse scan (pin 17, reLR = High, pin 18, reUD = High)

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	oC
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	According to typical value and tolerance in "ELECTRICAL CHARACTERISTICS"		
Input Signal			
PWM Duty Ratio	D	100	%

7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2 and all items are measured at the center point of screen except white variation. The following items should be measured under the test conditions described in 7.1 and stable environment shown in Note (5).

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Color Chromaticity	Red	Rx	θX=0°, θY =0° Grayscale Maximum	0.602	0.652	0.702	-	(1), (5)
		Ry		0.288	0.338	0.388	-	
	Green	Gx		0.274	0.324	0.374	-	
		Gy		0.557	0.607	0.657	-	
	Blue	Bx		0.103	0.153	0.203	-	
		By		0	0.048	0.098	-	
	White	Wx		0.263	0.313	0.363	-	
		Wy		0.279	0.329	0.379	-	
Center Luminance of White		LC		400	500	-		(4), (5)
Contrast Ratio		CR		700	1000	-	-	(2), (5)
Response Time		TR	θx=0°, θY =0°	-	13	18	ms	(3)
		TF		-	12	17	ms	
White Variation		δW	θx=0°, θY =0°	75	80	-	%	(5), (6).
Viewing Angle	Horizontal	θx+	CR≥10	85	89	-	Deg.	(1), (5)
		θx-		85	89	-		
	Vertical	θY+		85	89	-		
		θY-		85	89			

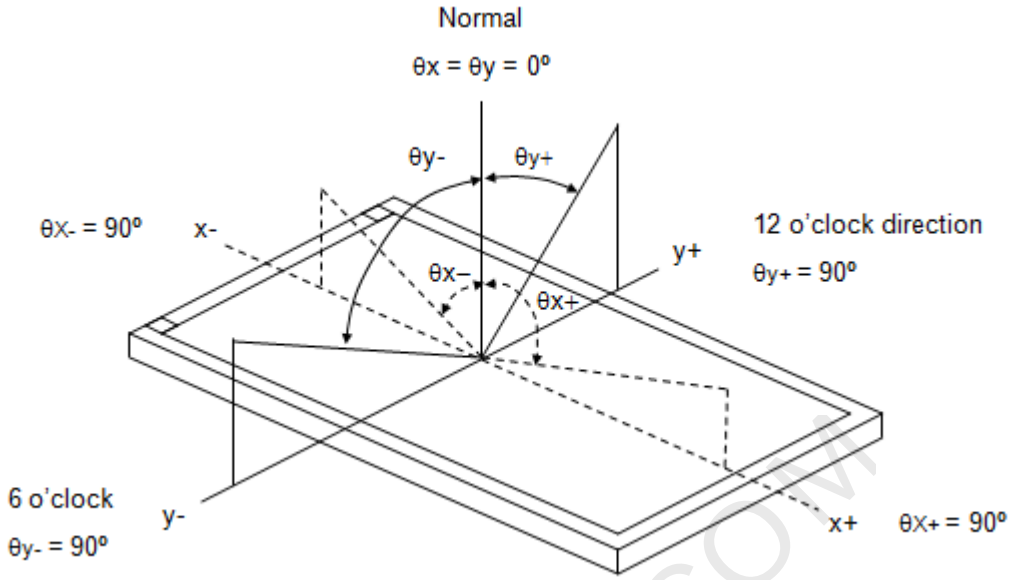
Definition：

Grayscale Maximum : Grayscale 255 (10 bits: grayscale 1023 ; 8 bits : grayscale 255 ; 6 bits: grayscale 63)

White : Luminance of Grayscale Maximum (All R,G,B)

Black : Luminance of grayscale 0 (All R,G,B)

Note (1) Definition of Viewing Angle (θx, θy):

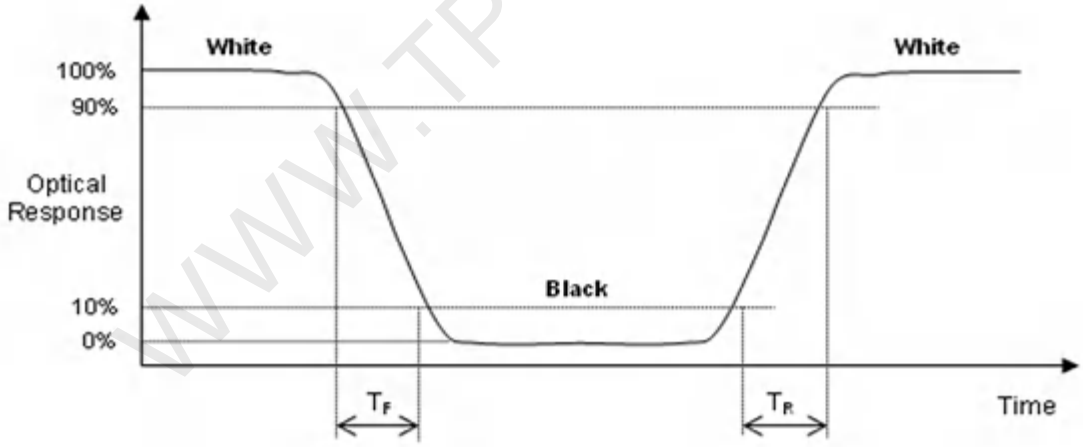


Note (2)Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = White / Black

Note (3)Definition of Response Time (T_R, T_F):

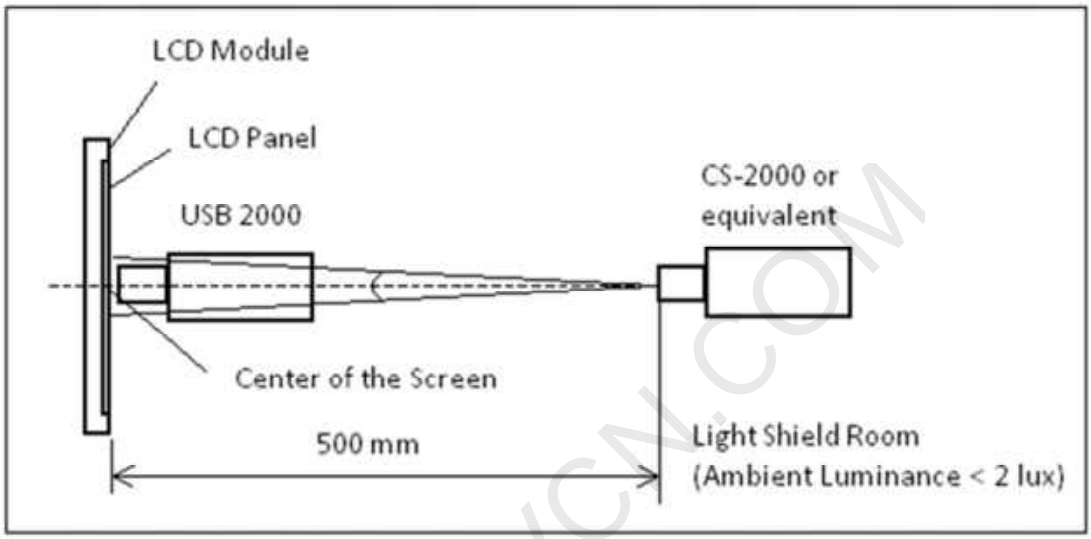


Note (4) Definition of Luminance of White (L_C):

Measure the luminance of White 255 at center point

Note (5) Measurement Setup:

The LCD module should be stabilized at given temperature to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 40 minutes in a windless room. The measurement placement of module should be in accordance with the module drawing.

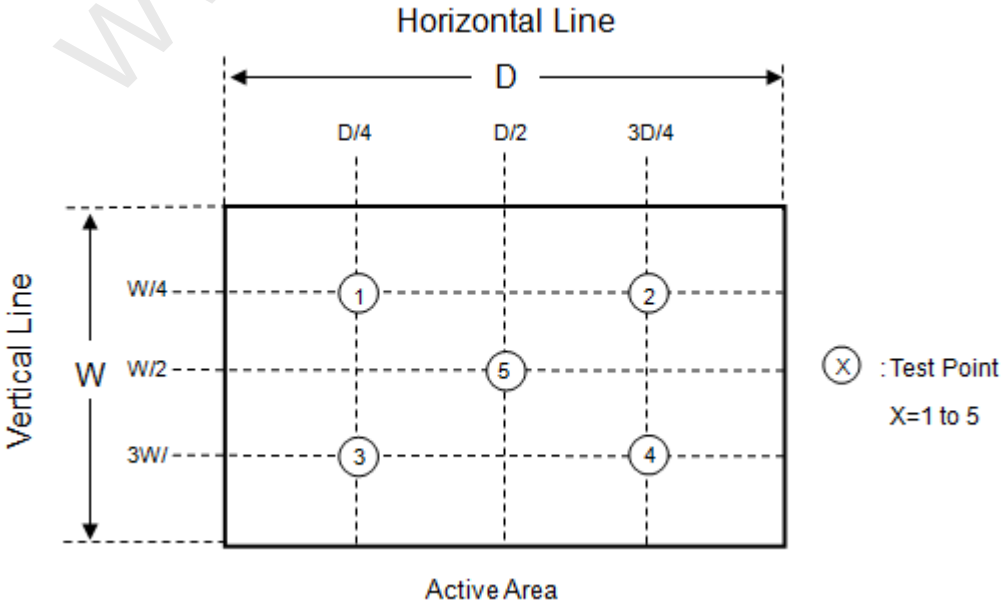


Note (6) Definition of White Variation (δW):

Measure the luminance of White at 5 points.

Luminance of White : L(X) , where X is from 1 to 5.

$$\delta W = \frac{\text{Minimum [L(1) to L(5)]}}{\text{Maximum [L(1) to L(5)]}} \times 100\%$$



8. RELIABILITY TEST CRITERIA

Test Item	Test Condition	Note
High Temperature Storage Test	80ºC, 240 hours	(1)(2) (4)(5)
Low Temperature Storage Test	-40ºC, 240 hours	
Thermal Shock Storage Test	-30ºC, 0.5hour←→80℃, 0.5hour; 1hour/cycle,100cycles	
High Temperature Operation Test	70ºC, 240 hours	
Low Temperature Operation Test	-30ºC, 240 hours	
High Temperature & High Humidity Operation Test	60ºC, 90%RH, 240hours	
ESD Test (Operation)	Contact Discharge: ± 8KV, 150pF(330Ω) Air Discharge: ± 15KV, 150pF(330Ω)	(1), (4)
Shock (Non-Operating)	200G, 2ms, half sine wave, 1 time for ± X, ± Y, ± Z.	(2)(3)
Vibration (Non-Operating)	1.5G, 10 ~ 300 Hz, 10min/cycle, 3 cycles each X, Y, Z	

Note (1)There should be no condensation on the surface of panel during test ,

Note (2) Temperature of panel display surface area should be 65ºC Max.

Note (3) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

Note (4) In the standard conditions, there is no function failure issue occurred. All the cosmetic specification is judged before reliability test.

Note (5) Before cosmetic and function test, the product must have enough recovery time, at least 24 hours at room temperature.

9. PACKAGING

9.1 PACKING SPECIFICATIONS

(1) 18pcs LCD modules / 1 Box

(2) Box dimensions: 465 (L) X 362 (W) X 314 (H) mm

(3) Weight: approximately 10.9Kg (18 modules per box)

9.2 PACKING METHOD

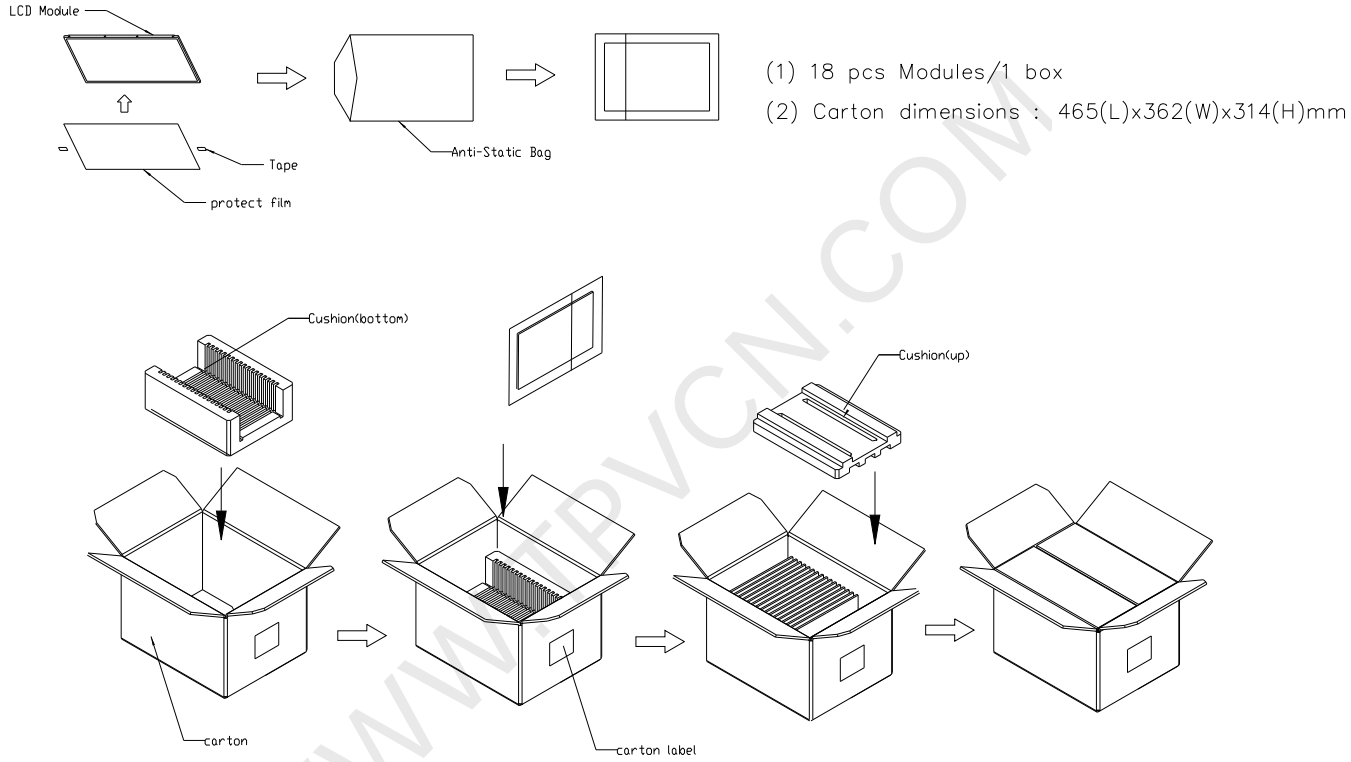
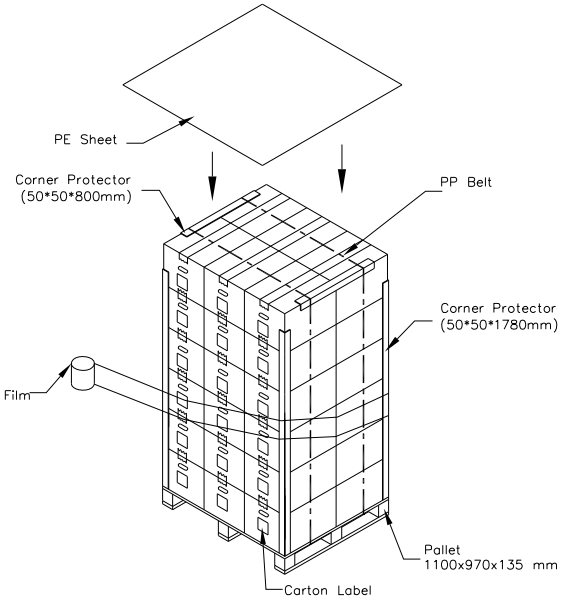


Figure. 9-1 Packing method

Sea / Land Transportation (40ft Container)



Air Transportation

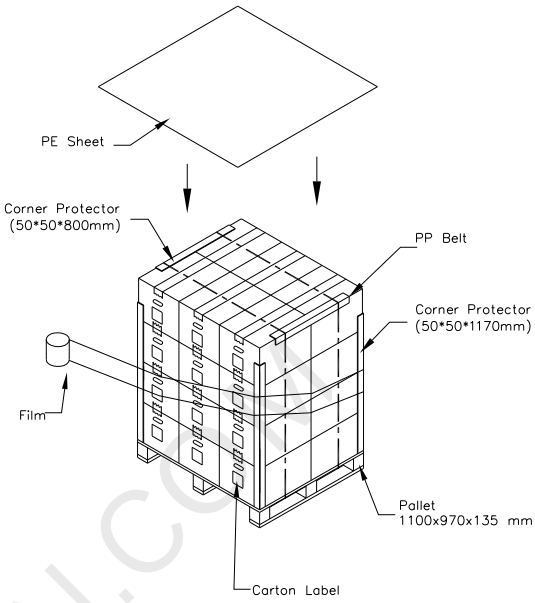
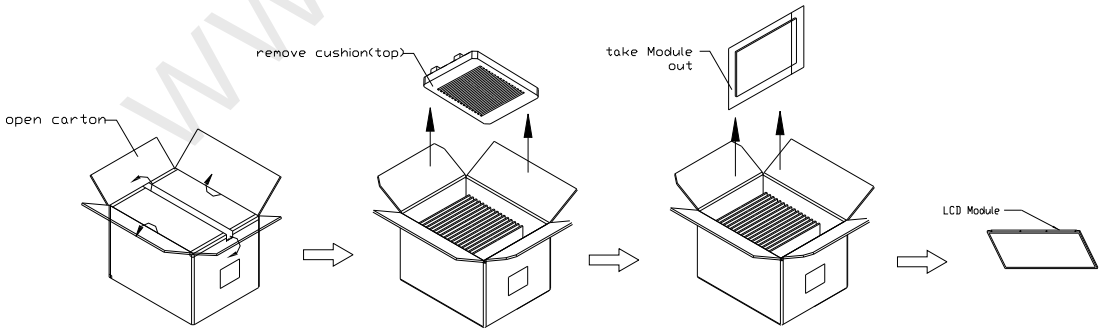


Figure. 9-2 Packing method

9.3 UN-PACKING METHOD



10. DEFINITION OF LABELS

10.1 MODULE LABEL

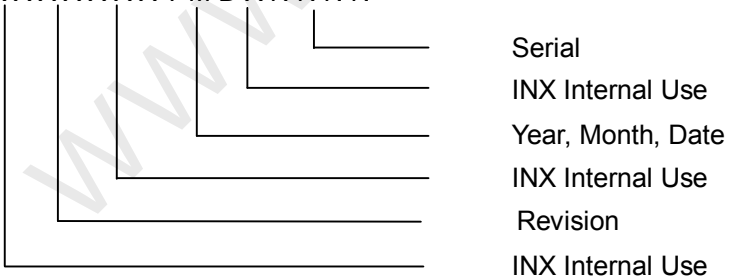
The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.

Note (1) Safety Compliance(UL logo) will open after C1 version.

(a)Model Name: G121XCE-L02

(b) ＊＊＊＊ : Factory ID

(c) Serial ID: X X X X X X X Y M D X N N N N



Serial ID includes the information as below:

(a)Manufactured Date: Year: 1~9, for 2021~2029

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I , O and U

(b)Revision Code: cover all the change

(c)Serial No.: Manufacturing sequence of product

11. PRECAUTIONS

11.1 ASSEMBLY AND HANDLING PRECAUTIONS

(1)The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.

(2)While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.

(3)Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.

(4)Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.

(5)If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.

(6)Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.

(7)If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.

(8)Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.

(9)Do not disassemble the module.

(10)Do not pull or fold the lamp wire.

(11)Pins of I/F connector should not be touched directly with bare hands.

11.2 STORAGE PRECAUTIONS

(1)When storing for a long time, the following precautions are necessary.

(a)Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5˚C and 30˚C at humidity 50+-10%RH.

(b)The polarizer surface should not come in contact with any other object.

(c)It is recommended that they be stored in the container in which they were shipped.

(d)Storage condition is guaranteed under packing conditions.

(e)The phase transition of Liquid Crystal in the condition of the low or high storage temperature will be recovered when the LCD module returns to the normal condition

(2)High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.

(3)It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.

(4)It may reduce the display quality if the ambient temperature is lower than 10 ºC. For example, the response time will become slowly, and the starting voltage of lamp will be higher than the room temperature.

11.3 OTHER PRECAUTIONS

(1) Normal operating condition

(a) Display pattern: dynamic pattern (Real display)

(Note) Long-term static display can cause image sticking.

(2) Operating usages to protect against image sticking due to long-term static display

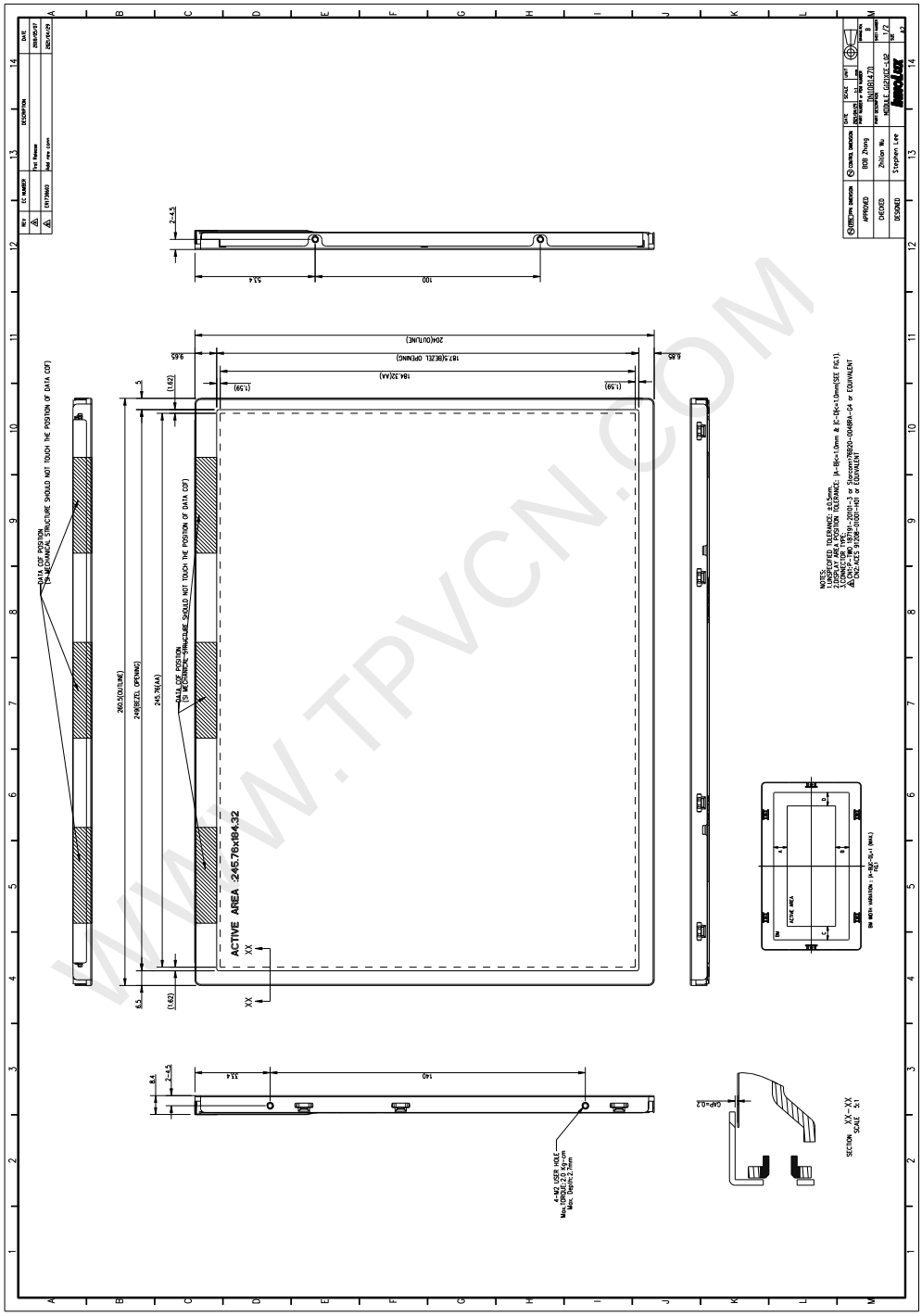
(a) Suitable operating time: under 16 hours a day.

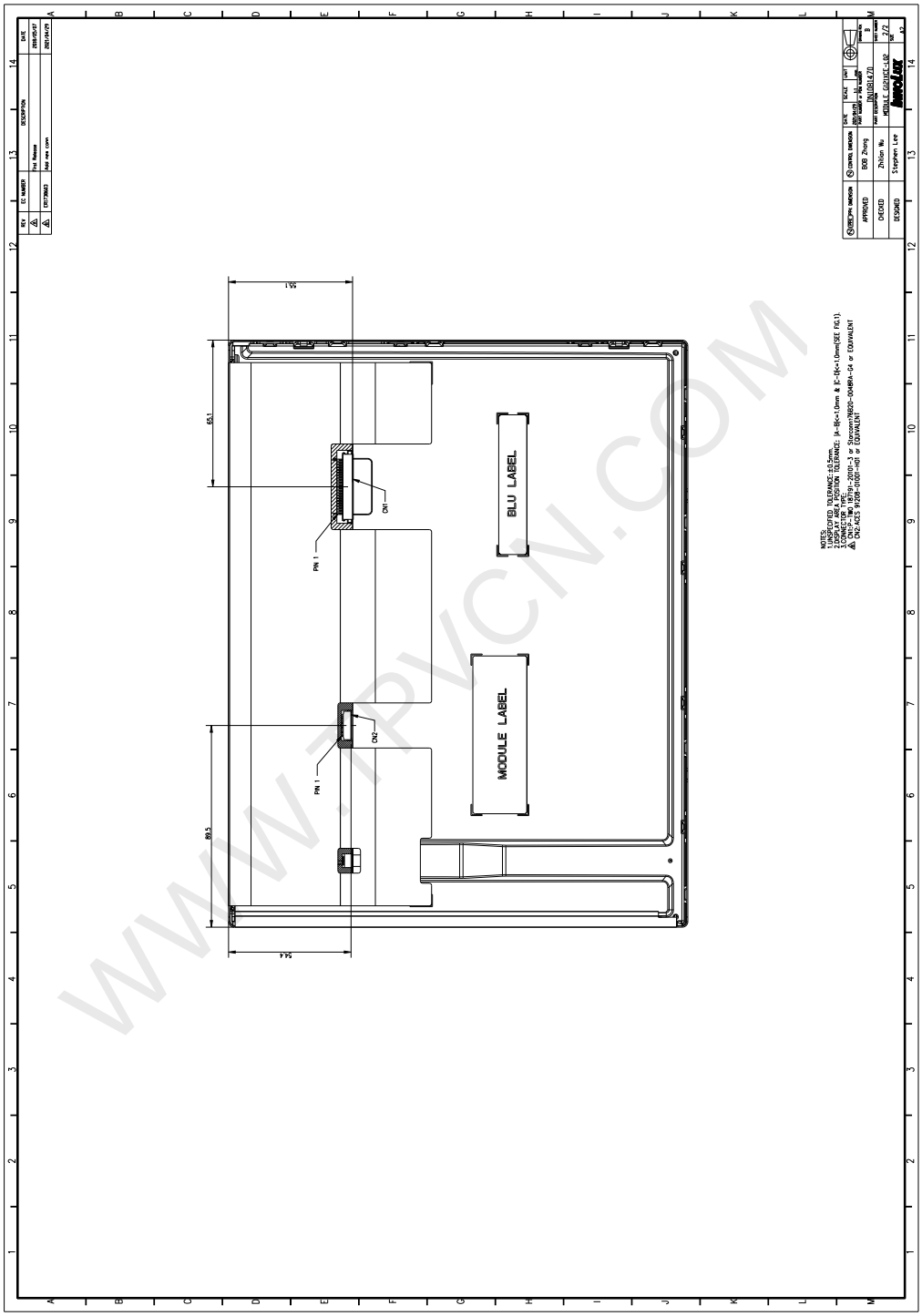
(b) Static information display recommended to use with moving image.

(c)Cycling display between 5 minutes' information(static) display and 10 seconds' moving image.

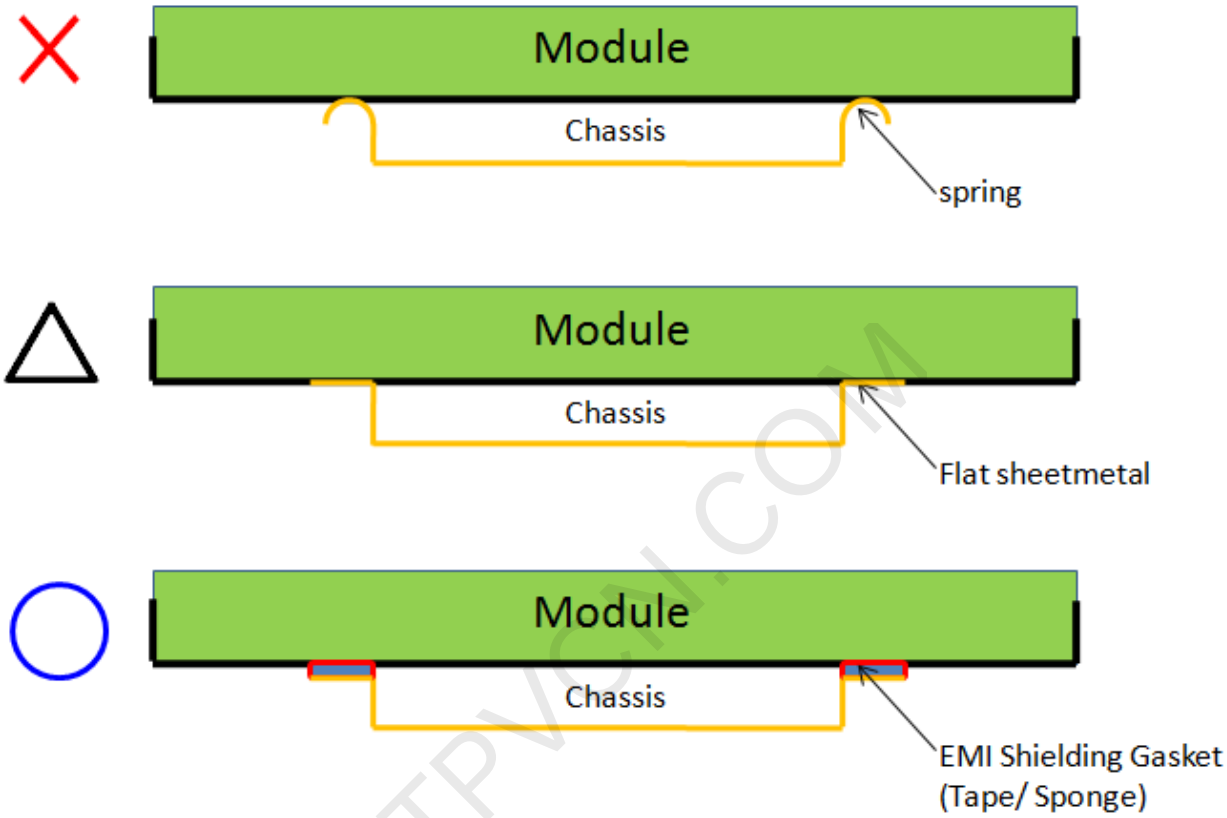
(3) Abnormal condition just means conditions except normal condition.

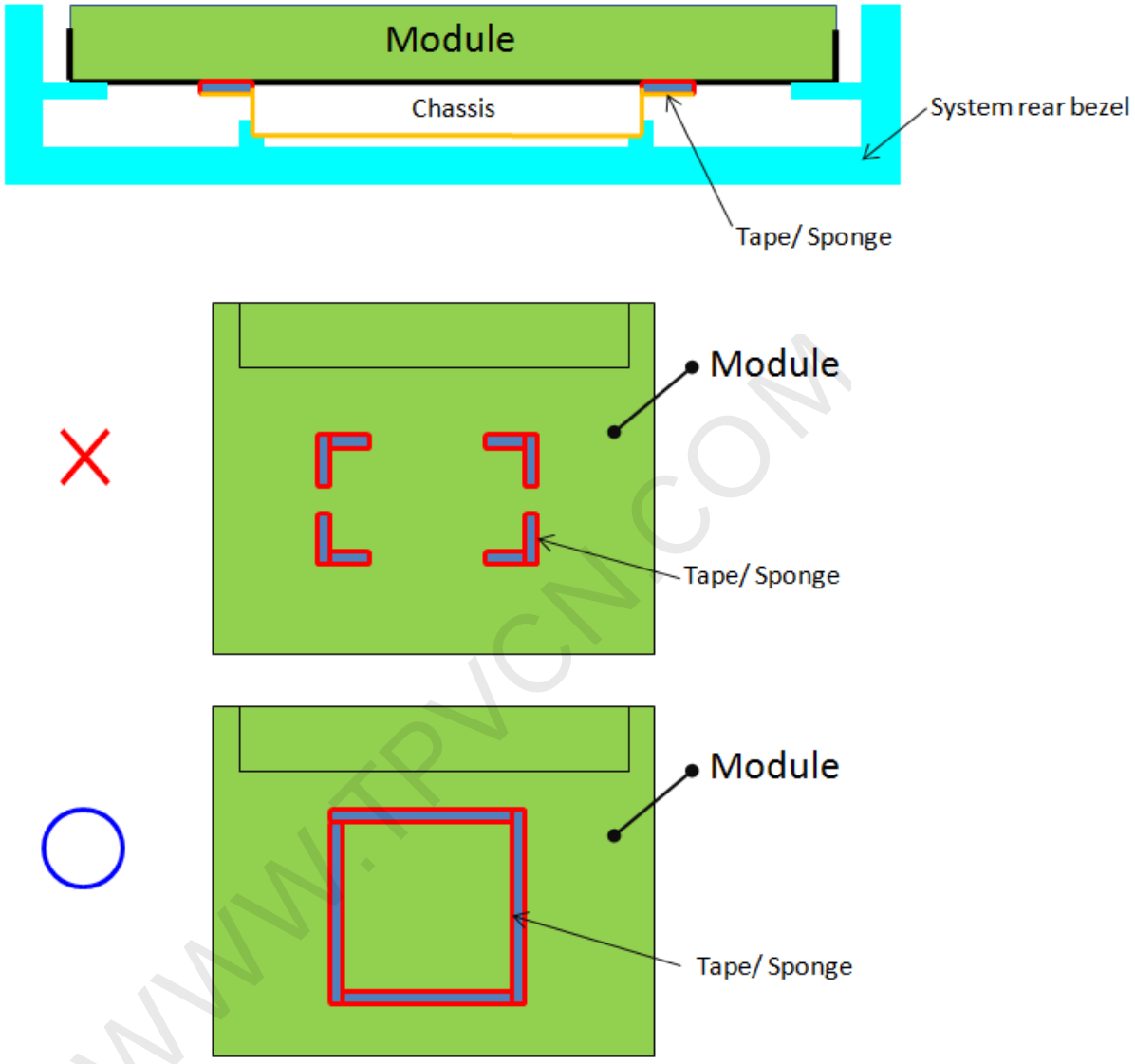
12. MECHANICAL CHARACTERISTICS

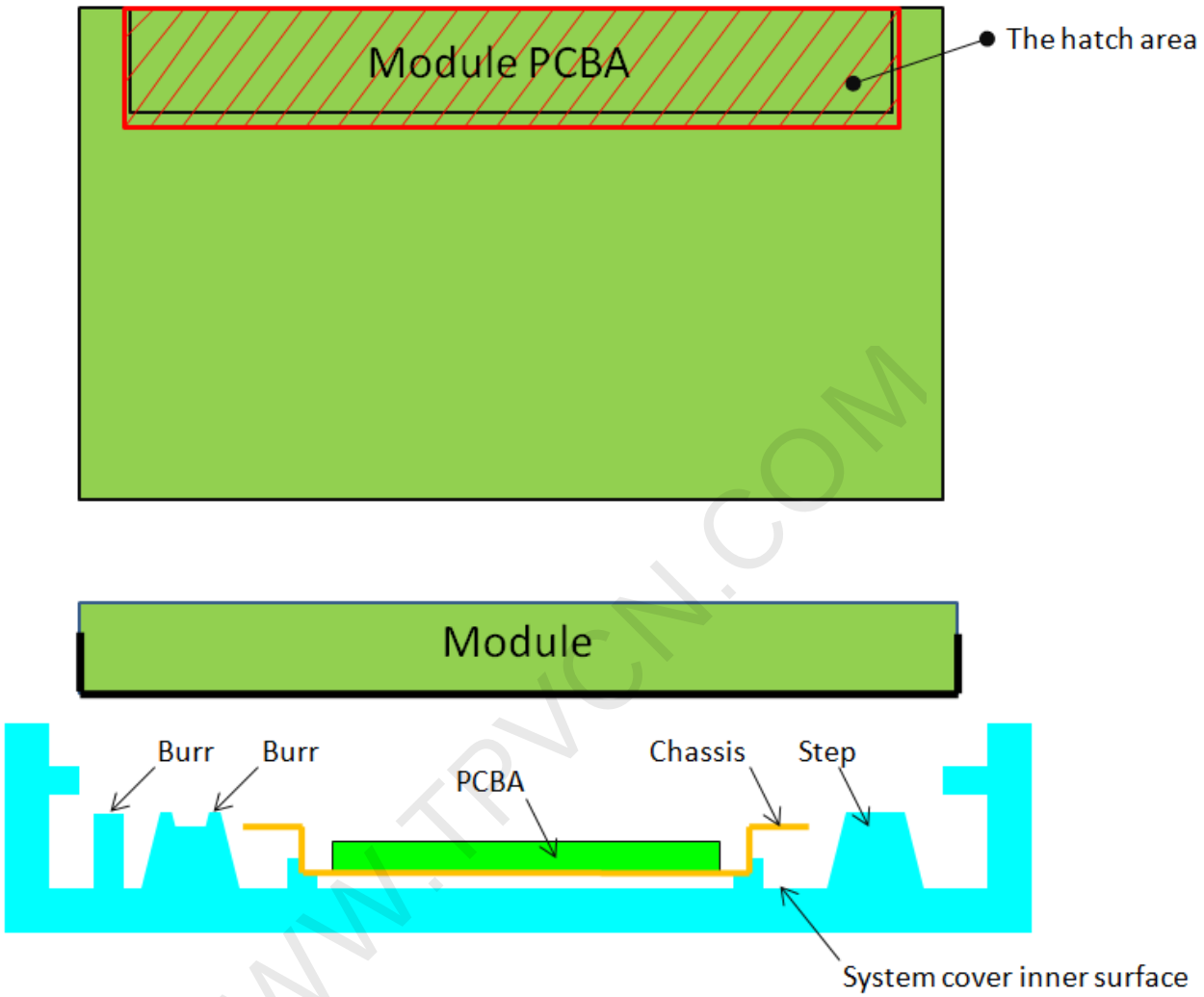


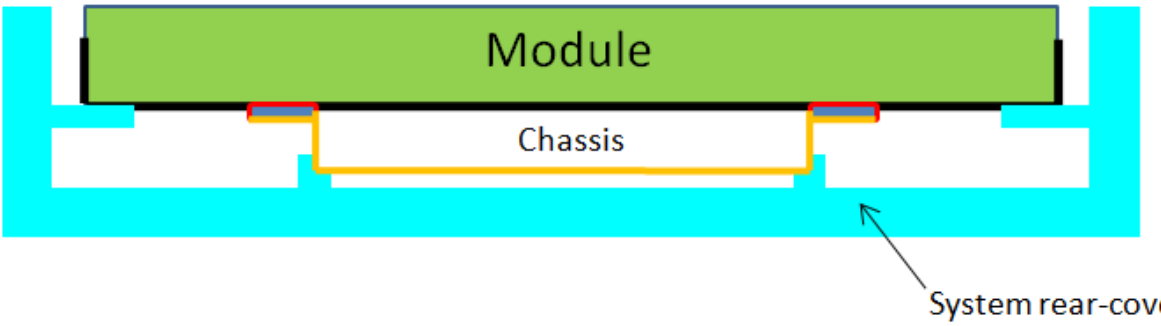


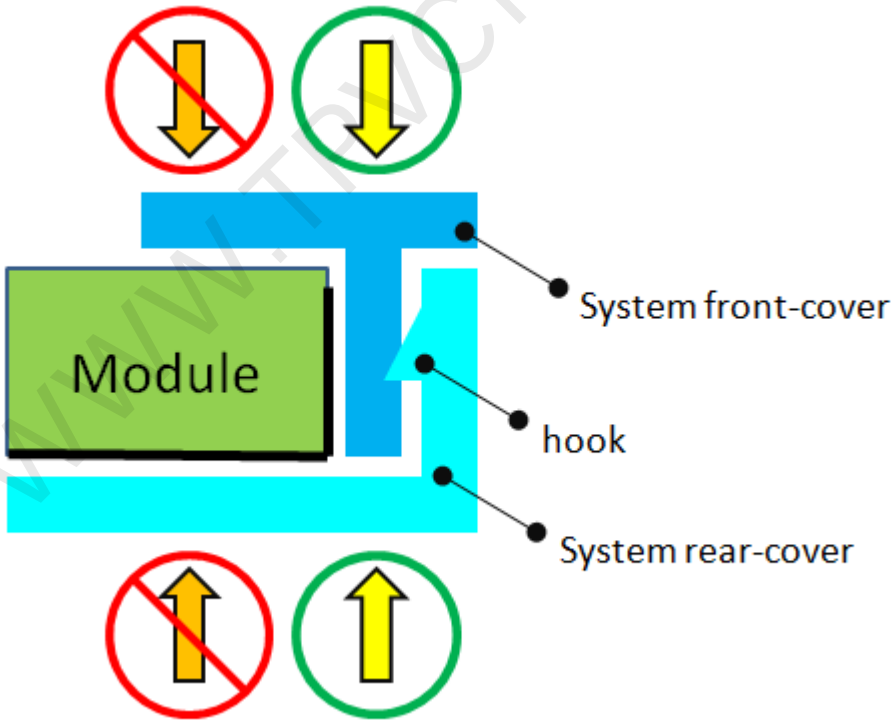
Appendix . SYSTEM COVER DESIGN NOTICE

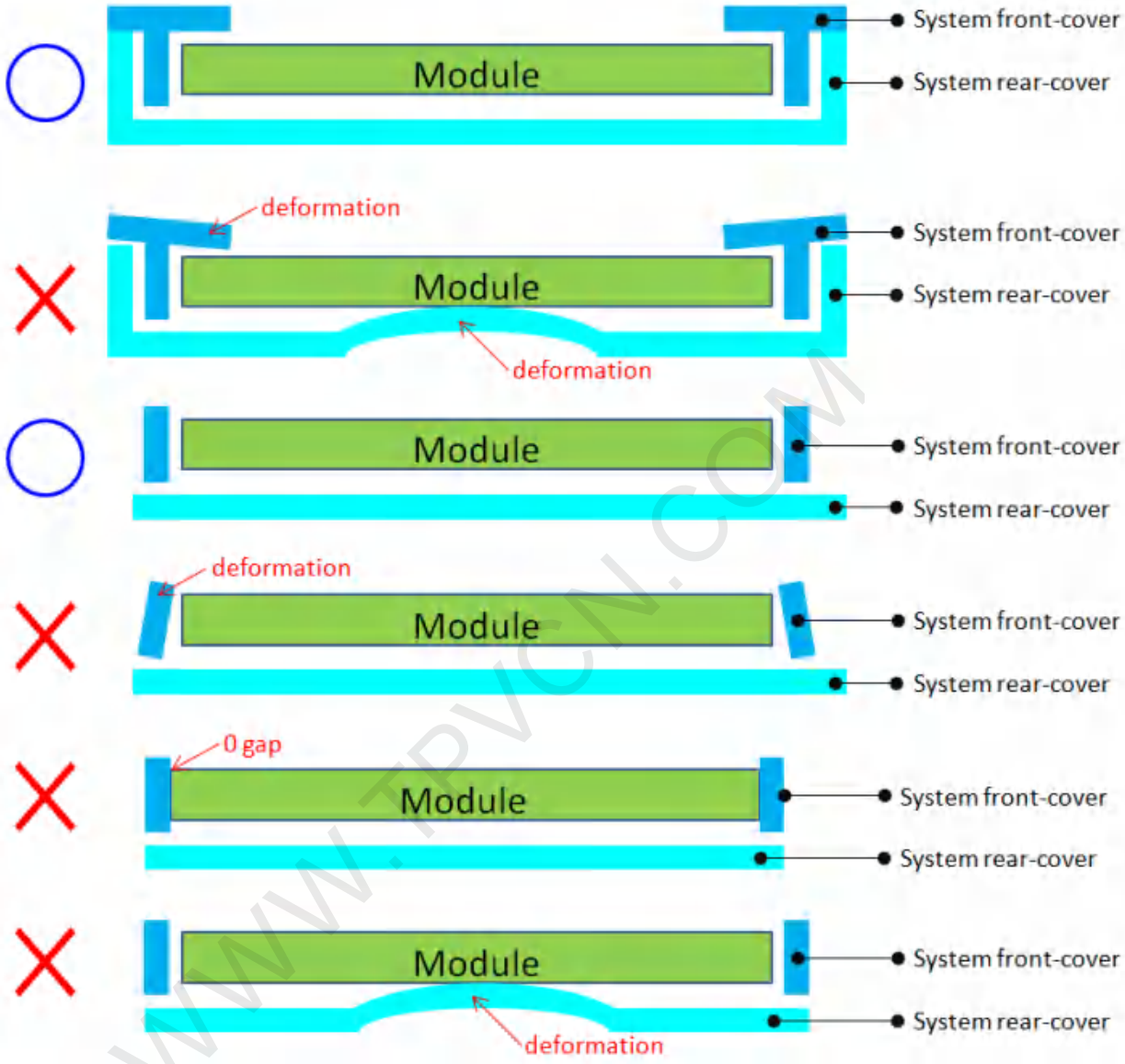
1	Set Chassis and IAVM Module touching Mode
	
Definition	a. To prevent from abnormal display & white spot after mechanical test, it is not recommended to use spring type chassis. b. We suggest the contact mode between Chassis and Module rear cover is Tape/Sponge, second is Flat sheet metal type chassis.

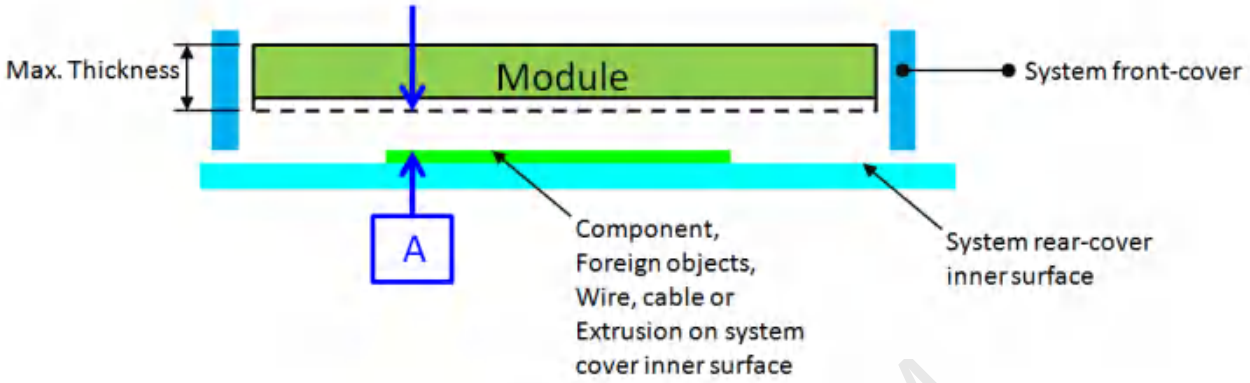
2	Tape/Sponge design on system inner surface
	
Definition	a. To prevent from abnormal display & white spot after mechanical test, we suggest using Tape/Sponge as medium between chassis and Module rear cover could reduce the occurrence of white spot. b. When using the Tape/Sponge, we suggest it be lay over between set chassis and Module rear cover. It is not recommended to add Tape/Sponge in separate location. Since each Tape/Sponge may act as pressure concentration location.

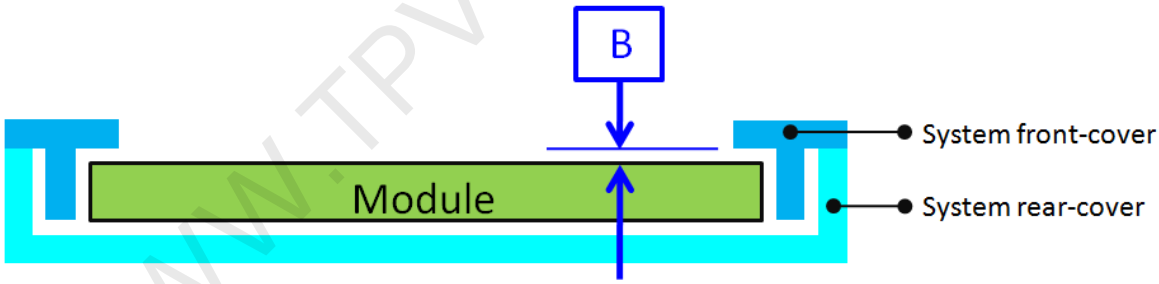
3	System inner surface examination
	
Definition	a. The hatch area on Module PCBA should keep at least 1mm gap(X,Y,Z direction) to any structure with system cover inner surface. b. Burr, Step, PCB protrusion may cause stress concentration. White spot may occur during reliability test.

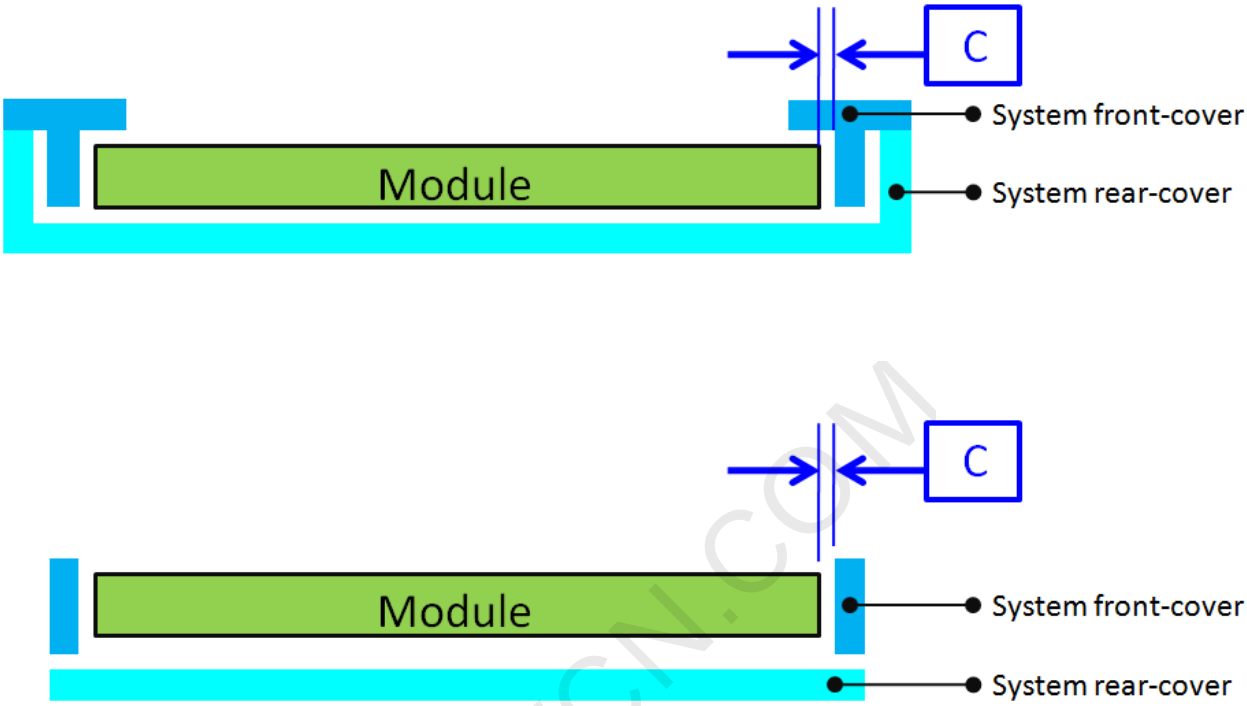
4	Material used for system rear-cover
	
Definition	System rear-cover material with high rigidity is needed to resist deformation during scuffing test, hinge test, pogo test or backpack test. Abnormal display, white spot, pooling issue may occur if low rigidity material is used. Pooling issue may occur because screw's boss position for module's bracket are deformed open-close test. Solid structure design of system rear-cover may also influence the rigidity of system rear-cover. The deformation of system rear-cover should not caused interference.

5	Assembly SOP examination for system front-cover with hook structure
	
Definition	To prevent panel crack during system front-cover assembly process with hook structure, it is not recommended to press panel or any location that relate directly to the panel.

6	Permanent deformation of system cover after reliability test
	
Definition	System cover including front cover and rear cover may deform during reliability test. Permanent deformation of system front cover and rear cover after reliability test should not interfere with panel. Because it may cause issue such as pooling, abnormal display, white spot and also cell creak. Note: If the interference cannot be avoided, please feel free to contract INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.

7	Design gap A between panel & any components on system rear-cover
	
Definition	System cover including front cover and rear cover may deform during reliability test. Permanent deformation of system front cover and rear cover after reliability test should not interfere with panel. Because it may cause issue such as pooling, abnormal display, white spot and also cell creak. Note: If the interference cannot be avoided, please feel free to contract INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.

8	Design gap B between system front-cover & panel surface
	
Definition	Gap between system front-cover & panel surface is needed to prevent pooling or glass broken. Zero gap or interference such as burr and warpage from mold frame may cause pooling issue near system front-cover opening edge. This phenomenon is obvious during swing test, hinge test, knock test or during pooling inspection procedure. To remain sufficient gap, design with system rib higher than maximum panel thickness is recommended. Note: If the interference cannot be avoided, please feel free to contract INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.

9	Design gap C between panel & system front-cover or protrusions
	
Definition	Gap between panel & system front-cover or protrusions is needed to prevent shock test failure. Because system front-cover or protrusions with small gap may hit panel during the test. Issue such as cell crack, abnormal display may occur. The gap should be large enough to absorb the maximum displacement during the test. Note: If the interference cannot be avoided, please feel free to contract INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.